CLAIMS

What is claimed is:

1. A method for conserving power, the method comprises:

measuring processing speed of at least a portion of an integrated circuit to produce measured processing speed;

comparing the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit; and

when the measured processing speed compares favorably to the critical processing speed, adjusting supply voltage to the integrated circuit to reduce power consumption of the integrated circuit.

2. The method of claim 1, wherein the measuring for the processing speed further comprises:

performing a function by the at least a portion of the integrated circuit;

counting at least one of a number of cycles of a known clock during the performing of function by the at least a portion of the integrated circuit and a number of repetitions of the function during a cycle of the known clock to produce a count value; and

equating the count value to the processing speed.

3. The method of claim 2, wherein the performing the function further comprises at least one of:

performing an add function;

performing a delay line function;

performing a memory retrieval function;

ring oscillation function; and

performing a multiplication function.

4. The method of claim 1, wherein the adjusting of the supply voltage further comprises:

determining a ratio between the measured processing speed and the critical processing speed; and

proportionally adjusting the supply voltage based on the ratio.

5. The method of claim 1, wherein the adjusting the supply voltage further comprises at least one of:

adjusting level of sensing the supply voltage for regulation of an on-chip DC-to-DC converter that produces the supply voltage; and

adjusting a reference voltage used for regulation of the on-chip DC-to-DC converter that produces the supply voltage.

6. The method of claim 1 further comprises:

periodically repeating the measuring, comparing, and adjusting to update the supply voltage.

7. The method of claim 1, wherein the at least a portion of the integrated circuit further comprises at least one of:

a speed test circuit;

a critical path of the integrated circuit; and

a replicated circuit of the critical path of the integrated circuit.

8. An apparatus for conserving power, the apparatus comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

measure processing speed of at least a portion of an integrated circuit to produce measured processing speed;

compare the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit; and

when the measured processing speed compares favorably to the critical processing speed, adjust supply voltage to the integrated circuit to reduce power consumption of the integrated circuit.

9. The apparatus of claim 8, wherein the memory further stores operational instructions that cause the processing module to measure the processing speed by:

performing a function by the at least a portion of the integrated circuit;

counting at least one of a number of cycles of a known clock during the performing of function by the at least a portion of the integrated circuit and a number of repetitions of the function during a cycle of the known clock to produce a count value; and

equating the count value to the processing speed.

10. The apparatus of claim 9, wherein the memory further stores operational instructions that cause the processing module to perform the function as at least one of:

performing an add function;

performing a delay line function;

performing a memory retrieval function;

ring oscillation function; and

performing a multiplication function.

11. The apparatus of claim 8, wherein the memory further stores operational instructions that cause the processing module to adjust of the supply voltage by:

determining a ratio between the measured processing speed and the critical processing speed; and

proportionally adjusting the supply voltage based on the ratio.

12. The apparatus of claim 8, wherein the memory further stores operational instructions that cause the processing module to adjust the supply voltage by at least one of:

adjusting level of sensing the supply voltage for regulation of an on-chip DC-to-DC converter that produces the supply voltage; and

adjusting a reference voltage used for regulation of the on-chip DC-to-DC converter that produces the supply voltage.

13. The apparatus of claim 8, wherein the memory further stores operational instructions that cause the processing module to:

periodically repeat the measuring, comparing, and adjusting to update the supply voltage.

14. The apparatus of claim 8, wherein the at least a portion of the integrated circuit further comprises at least one of:

a speed test circuit;

a critical path of the integrated circuit; and

a replicated circuit of the critical path of the integrated circuit.

15. A comprehensive system-on-a-chip comprises:

a processing core operably coupled to process input digital data and produce therefrom output digital data;

digital interface circuitry operably coupled to provide the input digital data to the processing core and to receive the output digital data from the processing core;

mixed signal circuitry operably coupled to convert input analog signals into the input digital data and to convert the output digital data into output analog signals; and

battery optimization circuitry that includes a DC-to-DC converter and a power conservation circuit, wherein the DC-to-DC converter is operably coupled to convert a battery voltage into a supply voltage that supplies at least one of: the processing core, the digital interface circuitry, and the mixed signal circuitry, wherein the power conservation circuit includes:

processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

measure processing speed of at least a portion of the comprehensive system-on-a-chip to produce measured processing speed;

compare the measured processing speed with a critical processing speed for the at least a portion of the integrated circuit; and

when the measured processing speed compares favorably to the critical processing speed, adjust supply voltage to at least one of the processing

core, the digital interface circuitry, and the mixed signal circuitry to reduce power consumption of the comprehensive system-on-a-chip.

16. The comprehensive system-on-a-chip of claim 15, wherein the memory further stores operational instructions that cause the processing module to measure the processing speed by:

enabling a function to be performed by the at least a portion of the comprehensive system-on-a-chip;

counting at least one of a number of cycles of a known clock during the performing of function by the at least a portion of the integrated circuit and a number of repetitions of the function during a cycle of the known clock to produce a count value; and

equating the count value to the processing speed.

17. The comprehensive system-on-a-chip of claim 16, wherein the memory further stores operational instructions that cause the processing module to enable the performing of the function as at least one of:

enabling performance of an add function;

enabling performance of a delay line function;

enabling performance of a memory retrieval function;

enabling performance of a ring oscillation function; and

enabling performance of a multiplication function.

18. The comprehensive system-on-a-chip of claim 15, wherein the memory further stores operational instructions that cause the processing module to adjust of the supply voltage by:

determining a ratio between the measured processing speed and the critical processing speed; and

proportionally adjusting the supply voltage based on the ratio.

19. The comprehensive system-on-a-chip of claim 15, wherein the memory further stores operational instructions that cause the processing module to adjust the supply voltage by at least one of:

adjusting level of sensing the supply voltage for regulation of the on-chip DC-to-DC converter; and

adjusting a reference voltage used for regulation of the on-chip DC-to-DC converter.

20. The comprehensive system-on-a-chip of claim 15, wherein the memory further stores operational instructions that cause the processing module to:

periodically repeat the measuring, comparing, and adjusting to update the supply voltage.

21. The comprehensive system-on-a-chip of claim 15, wherein the at least a portion of the comprehensive system-on-a-chip further comprises at least one of:

a speed test circuit;

a critical path of the comprehensive system-on-a-chip; and

a replicated circuit of the critical path of the comprehensive system-on-a-chip.